PATENT APPLICATION

Docket No.: 3902 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	DEAS, Alexander, Roger; ABROSIMOV, Igor Anatolievich
Serial No.:	10/038,868
Filed:	01/08/2002
Art unit:	2123
Confirmation No.	8180
Examiner:	Not assigned yet
For:	RECEIVER WITH AUTOMATIC SKEW COMPENSATION

Assistant Commissioner for Patents
Washington, D.C. 20231

August 28, 2003

PRELIMINARY AMENDMENT

Sir:

Prior to examination, please amend the above–identified application as follows:

IN THE CLAIMS:

Please substitute claims 1-33 with the following new claims:

1. A receiver for high speed data interconnect, comprising

- a sampling system for receiving a digital signal, comprising a plurality of samplers, for providing a series of signal copies of the received signal;

- a clock generator for generating clocks for spreading the samples in time so that each bit interval is covered by several samples,
- a transition detector for detecting the point in time where the input signal crosses the threshold;
- a controller for controlling the samplers, the controller tracking the eye of the eye diagram of the received signal using data obtained by transition detector;

wherein the sampler producing a signal having the lowest Bit Error Rate is selected based on BER distribution determined using BER values for different samplers, to define the sampler which is closest to the minimum in said BER distribution as the sampler used for data receiving.

2. A receiver according to claim 1, wherein the sampling system comprises at least one sampler coupled to a set of delays or a variable delay, for providing a series of spaced in time signal copies.

3. A receiver according to claim 1, wherein the sampling system comprises a plurality of samplers and a polyphase clock generator for generating multiple clock phases, for providing a series of spaced in time signal copies.

4. A receiver according to claim 1, wherein the sampling system comprises a plurality of samplers coupled to a set of delays, for providing a plurality of spaced in time signal copies.

5. A receiver according to claim 1, further comprising a logic network that compares the values of bit errors relative to each signal copy to select the signal copy with the minimum Bit Error Rate.

6. A receiver according to claim 1, wherein the signal copies are spaced in time uniformly.

7. A receiver according to claim 1, wherein the BER function is determined against RMS channel noise.

8. A receiver according to claim 1, wherein the continuous BER distribution is defined over multiple clock cycles in a series data stream.

9. A receiver according to claim 1, wherein several samplers are used in parallel with majority logic at the output.

10. A receiver according to claim 9, wherein BER is determined as follows, where n is the number of samplers:

$$BER_n(x) = \sum_{k=n+1}^{2n+1} C_{2n+1}{}^{k} \times \left[P^k(x) \times (1 - P(x))^{2n+1-k}\right]$$

11. A receiver according to claim 5, further comprising a means to determine the bit errors against the delay, a means to determine the delay corresponding to a copy with minimal bit error; and a means to apply the delay determined thereby to other samplers.

12. A receiver according to claim 1, wherein the sampler is implemented as register, flip-flop, latch, sample-hold, or track-and-hold device.

13. A receiver according to claim 1, further comprising a pipeline of latency adjustment elements.

14. A receiver according to claim 2, wherein said delay elements are incorporated in a data path, in a clock signal path, or in both paths.

15. A receiver according to claim 1, wherein the BER function is determined against the ratio of bit interval to RMS channel noise.

16. A receiver according to claim 15, wherein the required number of samplers is determined depending on the amount of channel noise.

17. A receiver according to claim 16, wherein the number of samplers per bit is from 14 to 20, preferably, 16.

18. A receiver according to claim 1, wherein at least one signal copy from the sampler is used to generate a feedback to control a source of threshold voltage to balance the number of ones and zeros in the sampled data.

19. A plurality of receivers according to claim 1, arranged on a plurality of parallel busses.

20. A method of high speed data interconnect, comprising:

- providing at least one sampler for sampling data, coupled with a set of delays or a variable delay;
- generating clocks for clocking the sampler or samplers at predetermined time intervals to provide a series of spaced in time signal copies covering at least one bit interval,

- tracking the eye of the eye diagram of the sampled signal; and
- selecting the sampler producing the signal having the lowest Bit Error Rate based on the BER distribution determined using BER values for different samplers, to define the sampler which is closest to the minimum in said BER distribution.

21. A method according to claim 20, wherein a plurality of samplers is clocked by multiple clock phases generated by a polyphase clock.

22. A method according to claim 20, wherein the data are sampled first and then, subsequently, the best time to have sampled that data is determined as the point where the BER function has its minimum.

23. A method according to claim 20, wherein the spaced in time signal copies are produced by using a set of delays or a variable delay, the step of combining signal copies comprises determining the bit errors against the delay and determining the delay corresponding to a copy with minimal bit error; wherein the step of sampling data is performed at a time corresponding to the delay determined thereby.

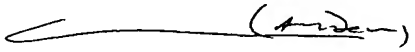
24. A method according to claim 20, wherein, further, the BER function is determined against the ratio of bit interval to RMS channel noise to define the number of samplers per bit.

25. A receiver according to claim 1 when used in a communication channel.

This Amendment cancels previous claims 1-33 and ads new claims 1-25. Entry and consideration of this Amendment is respectfully requested.

Enclosed please find three copies of the amended claims.

Respectfully submitted,

August 28, 2003  Alex Deas (alex@acuid.com)

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